Integrated Debug of Embedded Systems with the TLA700 Series Logic Analyzers

Overview

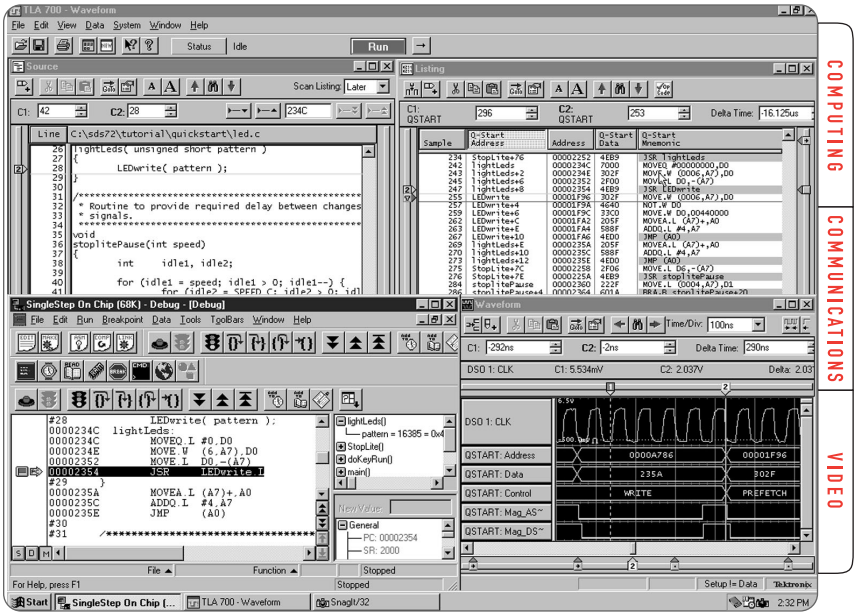

Figure 1. *With the Tektronix TLA700 Series Logic Analyzers, embedded system developers can easily combine source-level debug with run control and deep real-time trace, all on an open Windows® 95 PC platform.*

The Challenges of Modern Embedded System Debug

Throughout the past decade, embedded systems have grown exponentially in size and complexity, driven by the same silicon technology that has created low-cost, high-performance computers. Today's digital design team is being asked to develop embedded systems with increased functionality and higher performance in smaller packages at a lower cost, all under very aggressive development schedules. Fortunately, design tools have allowed developers to manage this increased complexity; however, on the other hand, developers are requiring increased performance and new capabilities from their debug tools to find those elusive problems that can cause delays and thereby disrupt the entire development schedule and threaten their product's time-to-market.

Recent developments in processor technology, both in terms of performance and complexity, have made a major impact on the tools used by the digital design team for both hardware and software debug. For the hardware developer, the most commonly used hardware debug tools are logic analyzers, oscilloscopes, and in-circuit-emulators (ICE). For the embedded software developer, the ICE has been the traditional tool-of-choice.

ICE technology provides three key debug capabilities to the digital design team:

- Source-level debug
- Processor run control
- Full-speed or real-time trace

With a classic ICE, these three capabilities are integrated into a single system. A hardware developer can use the ICE to start and stop the target system, read and modify registers and memory, and set breakpoints whenever visibility is needed into the internal operation of the target system. The embedded software developer can use the ICE to debug the code written using the ICE's source-level debugger while tracing the code as it executes in real-time while setting breakpoints when both control and visibility into internal processor operation are needed.

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Traditional ICE technology served digital design teams well during the 1980s and continues to offer excellent support for many of today's embedded processors. However, as processors continue their rapid advancement in performance and complexity, issues with the classic ICE began to surface:

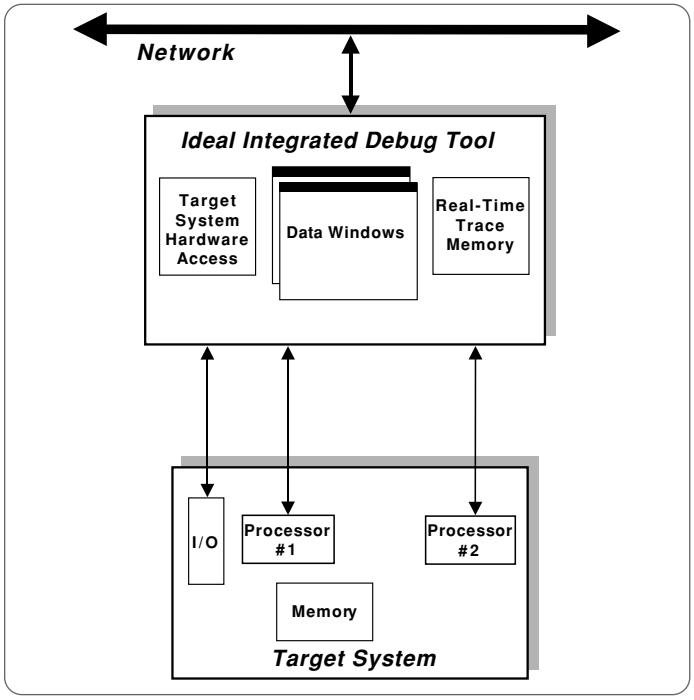
- Not only are they expensive to develop and deliver later in the processor's life cycle, they are high-priced and often require a fair amount of technical support to function correctly, especially with early prototype target systems.
- They are often developed for a fixed processor speed, which makes it difficult to scale in speed as the target processor is speed-enhanced.
- They often alter the circuit timing of the target system making them electrically intrusive.
- Support is often available for only a narrow range of target processor package styles, with bulky probe heads that make mechanical access to the target processor difficult, if not impossible.
- They don't offer the sophisticated triggering, high-speed timing, or analog analysis which is often critical for determining root cause of intermittent hardware problems.
- The latest advancements in processor technology, such as microprocessor cores embedded in ASICs which can create incredibly powerful solutions, have provided a correspondingly difficult debug challenge. Classic ICE technology provides no mechanism to debug these embedded cores.

These and other issues with the classic ICE forced processor vendors, tool vendors, and customers to consider a different approach. What's needed is a fresh approach to the problem of debugging modern digital designs featuring state-of-the-art processors that retained all of the advantages of the classic ICE with few or none of its drawbacks.

The Ideal Approach to Integrated Debug of Embedded Systems

The ideal tool strategy is for the digital design team to have both the hardware and software developers use the same set of tools. Additional benefits can be obtained if the support groups (manufacturing test, evaluation, service) can also use the same tools. Thus, test procedures can be developed once and used by everyone.

Traditionally, the hardware developers use DSOs, logic analyzers, and a classic ICE to debug the hardware. The software developers, on the other hand, start their software development on their PC or workstation and debug as much of the code as possible using the workstation's native mode compiler and debugger. When they've progressed as far as they can, they switch to a cross-compiler and a classic ICE to download code to the target system and debug it with the source-level software debugger while controlling the processor.

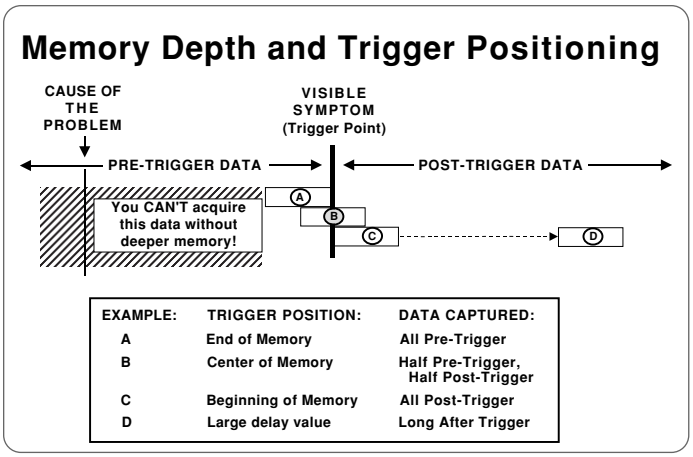


▶ ***Figure 2.*** *Components of an ideal embedded debug tool.*

Because the hardware and software developers are not using the same tools, it's often difficult to decide which debug tools to use when a hardware/software problem appears. Adding or removing debug tools often makes the problem disappear or changes the conditions that caused the problem. What's needed is an integrated set of debug tools that both the hardware and software developers can share to debug both the hardware and software in their target system.

Starting with a fresh design, an ideal solution for embedded system debug provides the following three key capabilities:

Open, Flexible, Platform Architecture. In today's rapidly changing development environment, digital design teams need the flexibility to adapt to new tools and capabilities. Nobody likes being at the mercy of a single vendor, so the ideal debug tool should offer the freedom to select individual best-of-class tools from any vendor. It should be based on an open platform architecture that not only runs all of these tools, but easily integrates into the development tool environment for file sharing and sharing of network resources such as printers, servers, and remote access.



▶ ***Figure 3.*** *Benefits of real-time deep memory trace.*

Source-level Debugger with Processor Run-control. In their quest for higher levels of performance, processor vendors have added sophisticated enhancement boosters including instruction pipelining/pre-fetch, instruction/data caches, internal clock multipliers, multiple execution units, and complex, external bus protocols. Unfortunately, these performance enhancements complicate the debug process.

An ideal debug tool supports these sophisticated processors with a hardware access mechanism that provides a complete set of control functions including start/stop run control, register/memory access, visibility of internal processor activities not visible at the external pins, and code download. It should be independent of the speed of the supported processor, electrically transparent, and support all of the mechanical styles within a processor family.

Such a debugger offers HLL source code support of optimized code, assembly language debugging, window-oriented display, variable values displayed in correct type and format, procedure trace back, instruction breakpoints, single-step execution, command macros, etc. Vendors often design their software debugger products to optimally work with a specific hardware access tool, with the benefit of high throughput, particularly with respect to code download speeds. An ideal solution would allow the digital design team to pick the best software debugger for their target processor and then choose the processor run-control tool that works best.

Deep Real-time Trace Memory. All digital systems are developed hierarchically; that is, the hardware developers typically work at the circuit and logic level where accurate signal timing and proper functional operation of the digital logic are required. Software developers, on the other hand, generally assume that the underlying hardware is functioning correctly and therefore develop at an assembly or high-level language level where proper functional operation of the software is required. Often times, however, when the underlying hardware is intermittent (e.g., metastable events) or when the software induces hardware faults (e.g., hardware sensitive to software data patterns), debug tools that "cross" domains are required.

A key advantage of the classic ICE is the full-speed or real-time trace capability that provides a history of the processor's execution – this proved invaluable for tracking down real-time cross-domain problems. During the debug of a difficult problem, the developers can trigger on the symptom, then look back in the trace memory to view the original cause of the problem. The deeper the memory, the farther back in time they can look (see Figure 3).

A key drawback of the classic ICE, however, is it's inability to provide high resolution timing or analog detail on key signals. Such a capability is critical in resolving those cross-domain problems. How often have team members come across an intermittent problem similar to this: the emulator used by the embedded software developer shows a problem in the code, but the code functions correctly? After consultation, the hardware developer then adds a logic analyzer or oscilloscope to the tool set in order to view the underlying signal detail, but then the problem disappears! What's needed is a tool that both the embedded software and hardware developer together can use to resolve these tough cross-domain problems by quickly and seamlessly moving from the high-level language (HLL) source code down to the underlying signals, all without either changing or adding more tools.

Another drawback of the classic ICE is its inability to run at full-speed with the latest processors. The classic ICE often inserts wait states or requires the developer to slow down the target system, thereby masking or obscuring real-time problems that intermittently surface. The ideal debug tool operates at full-speed or real-time with the target system processor.

Many of the package styles used in today's embedded systems such as Quad-Flat-Pack (QFP) or Ball-Grid-Array (BGA) don't have the mechanical clearance for multiple probe connections. An ideal debug tool provides as many measurements as possible – all through a single probe connection – such as analog, high-speed timing, state, disassembly, HLL source code, and performance analysis. Besides the obvious mechanical benefits, a key benefit of a single probe connection is minimal electrical intrusiveness, which prevents the debug tool from masking intermittent problems.

An ideal debug tool also has the ability to correlate events between multiple processors. Today's target systems often have multiple processors, each with a specifically assigned set of system tasks. Troubleshooting intermittent problems often requires correlating data flow between processors to see which one is causing the problem. What's required is a debug tool that can automatically time-correlate data from multiple processors and accurately display the acquired data side-by-side. Especially with deep memory data from two or more processors, the ideal tool accurately displays the correlated data as it occurs on the target system, from the first sample to the Nth sample – there should be no drift between samples throughout the acquisition.

The ideal debug tool also supports other processors at an incremental cost – no need to invest in completely new tools. It also supports new processors as soon as they are announced by the processor vendor.

The Tektronix Integrated Debug Solution

By combining an open, flexible platform architecture upon which best-of-class source-level debuggers with run control can be installed in addition to a logic analyzer with its deep real-time deep trace memory, Tektronix' Integrated Debug solution approaches the ideal debug tool mode. Tektronix' Integrated Debug Solution enables the digital design team to assemble debug solutions for meeting the challenges of today's as well as tomorrow's sophisticated processors.

Open, Flexible, Platform Architecture. By building upon an industry-standard PC computer and Windows® 95 operating system, instead of a proprietary, closed computer environment found on older logic analyzers, the TLA700 Series provides an open, flexible platform environment that offers the digital design team a choice. Now the digital design team has a tool that all team members know how to operate – no proprietary user interface or arcane commands to understand. They can select the best software debugger and run-control probe and install them directly on the TLA700 for a single, integrated debug tool. By supporting an open standard, the TLA700 Series allows the developer to take advantage of industry advancements in on-chip emulation functionality and performance.

Tektronix works closely with the leading processor vendors to ensure that processor support is available as soon as the processor hits the market. Support for additional processors is available at an incremental cost – no need to invest in completely new tools.

Finally, the TLA700's Windows 95-based PC easily integrates into the team's development tool environment for sharing files and network resources such as printers, servers, and remote access.

Source-level Debugger with Processor Run-control. Processor vendors and industry experts agree that the future of embedded system debug for today's sophisticated processors lies with on-chip emulation. This capability, otherwise known as Background Debug Mode (BDM), On-Chip-Emulation (ONCE), and JTAG, puts basic debugging functions directly on the processor chip. Access is provided through a small set of pins (typically less than eight pins), otherwise known as an N-wire interface, to which a low-cost run-control probe is connected that provides a connection for the software debugger running on a host computer. Functions include start/stop run control, register/memory access, visibility of internal processor activities not visible at the external pins, and code download.

With the electrical transparency of on-chip emulation, the processor operates at full speed since there's none of the electrical intrusiveness associated with the classic ICE. Furthermore, internal accesses are made visible that never appear on the processor's external bus. Finally, since the mechanical interface is through a simple connector, all mechanical package styles within a processor family are supported.

Often coupled with the on-chip emulation capability is a software debugger that works with high-level languages such as Ada or C++ that runs on a computer separate from the target system. The debugger takes the file from the compiler/assembler/linker and loads onto the target system for execution. The debugger is used to control the execution (e.g., start/stop, start at an address, break execution at an address, or variable access) and to monitor the execution (e.g., variable and stack tracking). Coupled with the on-chip emulator, the software debugger performs all of the functions of the classic ICE, except for real-time trace that is provided by the TLA700 Series logic analyzer.

Most software debuggers come with a recommended on-chip emulation interface to the processor in the target system, often in the form of a run-control probe. These run-control probes come in a variety of interfaces to the PC (parallel, serial, or LAN) and a range of performance capabilities, particularly for code-download speed. After you've selected your software debugger, select the run-control probe that the software debugger vendor recommends

The TLA700 Series offers a complete debug package. If the embedded software developer selects a PC Windows-based software debugger, then the debugger can operate directly on the TLA700. The run-control probe can be connected via the parallel port, serial port, or over LAN. The developer can run the other software tools (compiler, editor, etc.) directly on the TLA700 or access them over the network. The source and object files are readily available through a network file system.

Deep Real-time Trace Memory. The primary advantage of a logic analyzer is its real-time acquisition, which can acquire every event on the target system at full speed. Coupled with deep memory, the developer can look back in time at the events leading up to the symptom of a problem, thereby seeing the root cause of the problem. All other things being equal, the deeper the memory, the farther back in time the developer can look to view the root cause of a problem.

The TLA700 Series is a family of logic analyzers with a state-of-the-art real-time acquisition system based upon the patented MagniVu™ acquisition technology. MagniVu provides 500 ps timing resolution simultaneous with 200 MHz state on all channels, all through a single probe. The TLA700 Series also features a 1 GHz bandwidth digitizing oscilloscope (DSO) module with 5 GS/s simultaneously on all channels which provides an analog view that is automatically time-correlated with all data from the logic modules.

With the HLL source code support that comes standard on the TLA700, the embedded software developer can view the source code as written in one window and the code as executed by the target system's processor in another window. Similar to a software debugger, the developer can step forward or backward through the source code and view the underlying disassembled data that was acquired or vice versa. The TLA700's HLL source code support is a non-intrusive tool that does not require any change to the software compilation process other than requiring that the compiler's debug mode is enabled. It's a universal tool that supports any high-level language whose compiler produces supported object file formats including IEEE695, OMFx86, COFF, Elf/Dwarf, Elf/Stabs, and ASCII.

An unlimited number of symbols and ranges are supported. Once loaded into the TLA700's symbol database, these symbols are available to all of the TLA700's tools including HLL source code support, performance analysis, disassembly, and logic analyzer trigger setup. The TLA700's HLL source code support complements your favorite source-level debugger by displaying actual executed instructions acquired in real-time from the target system processor's bus.

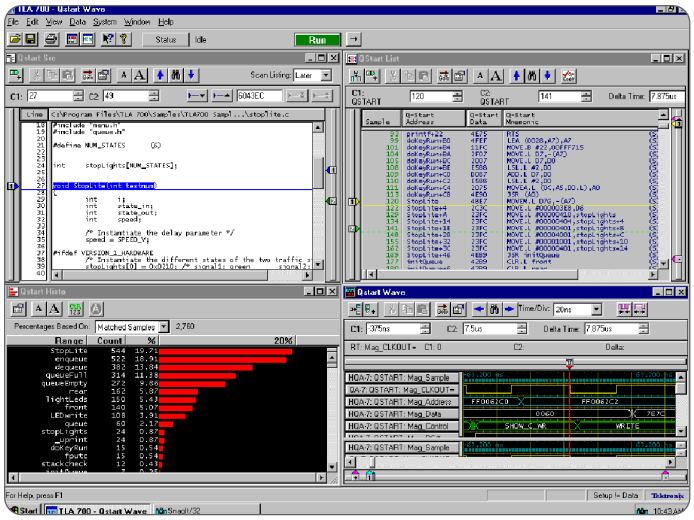
The TLA700 can easily and automatically correlate data from up to five processors – there's no need to trade memory depth for timestamps that are required for data correlation by older logic analyzers. Due to its modern platform architecture, the TLA700 uses a master system clock to which the local clock on each acquisition module is aligned, as compared to older architectures with local clocks that drift apart, especially with deep trace memories. The key benefit of this approach is that each sample on each module is locked together, whether it's the first sample or the Nth sample – there's no drift between data from multiple modules.

With the TLA700 Series logic analyzer, coupled with its HLL source code support, both hardware and embedded software developers can share the same debug tool. The embedded software developer can view the symptom of a problem at the HLL source code level; then, the hardware developer, using the same debug tool, can view the underlying signal detail with 500 ps timing resolution or view key signals with the 1 GHz scope module – no need to change debug tools.

Benefits of Tektronix' Integrated Debug

Among the many benefits of Tektronix' Integrated Debug approach to embedded systems development:

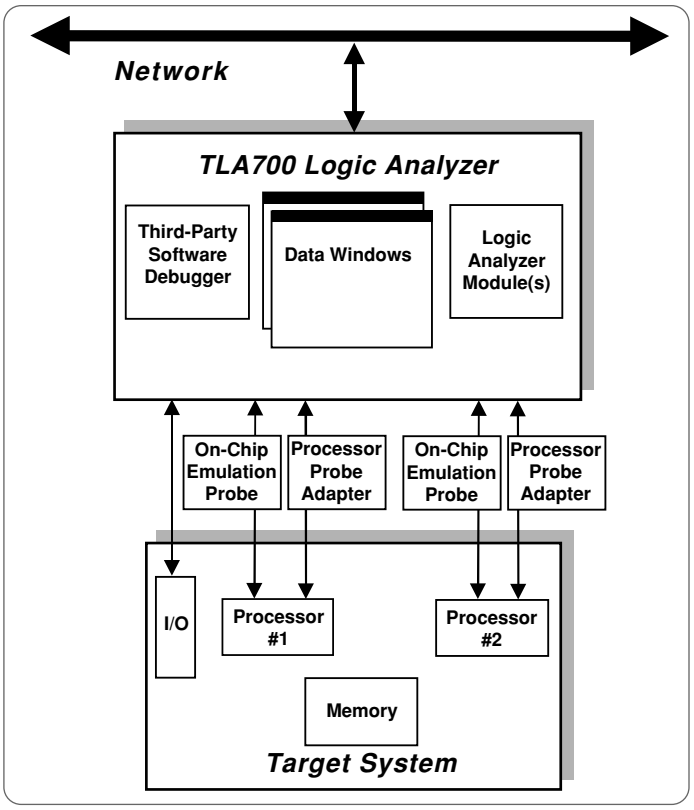
Source-level Debugger with Processor Run Control and Deep Real-time Trace – All in One Integrated Package. Unlike other logic analyzers that depend upon a closed, proprietary environment, the TLA700 provides all of this capability in a single package, based upon an open, integrated PC running Windows 95. You can load your favorite PC-based software debugger with on-chip emulation support onto the TLA700 and operate it concurrently, all under the same user interface. By coupling the real-time capabilities of the TLA700 with the on-chip emulation capabilities of the latest processors, you now have the functionality of a classic ICE that can easily keep pace with the fastest processors. The TLA700's 200 MHz state acquisition rate has plenty of headroom to easily satisfy the high speeds required by the external buses of today's most advanced processors. Not only is it easy to configure and quick to get up and running, you save valuable bench and desk space. Furthermore, since the TLA700 is inherently networkable, it's easy to connect your entire digital design team across the LAN.



▶ ***Figure 4.*** *Viewing the big picture of overall target system behavior from individual signals to high-level language source code on the TLA700 Series logic analyzer.*

View the Big Picture of the Target System – From Signals To Source Code. The TLA700 logic analyzer coupled with a software debugger coupled to an on-chip emulator provides a unique benefit that is not available with the classic ICE – the ability to view both timing and analog detail. The power of the TLA700 lies in its inherent ability to acquire data from the analog, timing, and state levels in the target system and present an integrated "big picture" view of the target system's operation. With the TLA700 Series as the foundation of your integrated debug solution, you get the debugging capabilities of a classic ICE plus the ability to trace bus activity, thereby allowing you to look back in time to the underlying root cause of the problem. You can trace the symptom of an intermittent problem at the HLL source level, and drill all the way down to the underlying signal detail with 500 ps timing resolution provided by the LA module or 200 ps analog resolution provided by the DSO module.

Both hardware and software developers on the digital design team can share the same debug tool. The HLL source code support is integrated and comes standard with every TLA700 – no need to buy optional tools or software packages (see Figure 4).



▶ ***Figure 5.*** *Third-party source-level debuggers with run-control coupled with the TLA700's deep real-time trace with high-speed timing and analog acquisition, all based upon the TLA700's open Windows 95 PC platform.*

Early Processor Support – Including Support for Embedded Core Processors. When the latest processor hits the market, you usually have to wait a long time for an ICE. With the TLA700, Tektronix works closely with processor vendors to ensure that support is available when the latest processor hits the market. Now, you can begin to debug your embedded system early and quickly to meet your time-to-market objectives.

When it comes to embedded core processors, there are no classic ICE solutions. Fortunately, the TLA700 can support embedded core processors provided the developer exposes those signals that are required by the TLA700's disassembler.

With the classic ICE, every time you change processors or go to the next speed grade, you are forced to buy a new ICE. With the TLA700 logic analyzer, you get support for up to 200 MHz state operation which provides plenty of headroom for today's and tomorrow's fastest processors. If you change to a faster processor, you can often use the same probe adapter since the TLA700's processor support is designed to work over a wide range of processor speeds. When you change processors or processor families, the only thing you need to change on your TLA700 is the processor probe adapter and the setup software. Thus, you maintain your investment in the TLA700, thereby lowering your overall total cost of ownership.

Putting Tektronix' Integrated Debug Solution to Work. For an integrated debug solution for your embedded target system, a complete setup can be assembled by following three simple steps. This configuration lets you download code, set both hardware and software breakpoints, start the processor, access and change registers and memory and trace your code in real-time (see Figure 5):

1. Start with your favorite third-party software debugger and their recommended run-control probe and install it on the TLA700's open Windows 95 PC platform.
2. Add the appropriate processor support which consists of a processor probe adapter that connects to your processor and setup software which configures your TLA700 to acquire and disassemble data from your target system.
3. Use the TLA700 Series logic analyzer for the deep real-time trace. Its card modularity lets you add additional logic analyzer channels or DSO channels.

Conclusion

As processors get even more complex and the shift to on-chip emulation support for many processors continues, Tektronix can help minimize the risks while maximizing your team's productivity. With the Integrated Debug solution provided by Tektronix as the foundation for your debug needs, you get the debugging capabilities of a classic ICE plus the strengths of a logic analyzer, including high-speed timing and analog analysis, all in one integrated package with complete support for the transition to integrated debug.

Contact Tektronix:

ASEAN Countries & Pakistan (65) 6356 3900

Australia & New Zealand (65) 6356 3900

Austria +43 2236 8092 262

Belgium +32 (2) 715 89 70

Brazil & South America 55 (11) 3741-8360

Canada 1 (800) 661-5625

Central Europe & Greece +43 2236 8092 301

Denmark +45 44 850 700

Finland +358 (9) 4783 400

France & North Africa +33 (0) 1 69 86 80 34

Germany +49 (221) 94 77 400

Hong Kong (852) 2585-6688

India (91) 80-2275577

Italy +39 (02) 25086 1

Japan (Sony/Tektronix Corporation) 81 (3) 3448-3111

Mexico, Central America & Caribbean 52 (55) 56666-333

The Netherlands +31 (0) 23 569 5555

Norway +47 22 07 07 00

People's Republic of China 86 (10) 6235 1230

Poland +48 (0) 22 521 53 40

Republic of Korea 82 (2) 528-5299

Russia, CIS & The Baltics +358 (9) 4783 400

South Africa +27 11 254 8360

Spain +34 (91) 372 6055

Sweden +46 8 477 6503/4

Taiwan 886 (2) 2722-9622

United Kingdom & Eire +44 (0) 1344 392400

USA 1 (800) 426-2200

For other areas contact Tektronix, Inc. at: 1 (503) 627-7111

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